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09/424,667 **PATENT** CJC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 7,100,086

Issue Date: August 29, 2006

Inventor(s): Makoto KUDO; Yoichi HIJIKATA

Title: MICROCOMPUTER, ELECTRONIC EQUIPMENT AND DEBUGGING SYSTEM

Docket No.: 104822

REQUEST FOR CERTIFICATE OF CORRECTION UNDER RULE 322

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is respectfully requested that a Certificate of Correction be issued in order to correct the errors specified in the attached copy of Certificate of Correction Form PTO-1050.

It is believed that the errors are on the part of the Patent and Trademark Office, and therefore no fee is due in relation to this matter in accordance with the provisions of 37 C.F.R. §1.322. However, should any fee be due, please charge the same against Deposit Account No. 15-0461 in order to ensure prompt issuance of a Certificate of Correction.

Respectfully submitted,

Dinnatia Doster-Greene

James A. Oliff
Registration No. 27,075

Dinnatia J. Doster-Greene
Registration No. 45,268

JAN 16 2007

JAO:DJG/jfb

Date: January 10, 2007

OLIFF & BERRIDGE, PLC
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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,100,086

DATED : August 29, 2006

INVENTOR(S) : Makoto KUDO; Yoichi HIJIKATA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims, columns 17-22, please replace claims 1-36 with the claims listed below, which were submitted to the U.S. PTO with the Supplemental Amendment filed December 1, 2003.

1. A microcomputer having an on-chip debugging function, comprising:
a central processing unit for executing instructions; and
a first monitor section which performs data transfer to and from a second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, said second monitor section being provided outside said microcomputer and performing a processing to convert a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, said first monitor section includes a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization, and a circuit for sending and receiving data based on said first sampling clock, said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

2. The microcomputer according to claim 1, said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

3. The microcomputer according to claim 1, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

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4. The microcomputer according to claim 2, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on the memory map in the debugging mode.

5. The microcomputer according to claim 1, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

6. The microcomputer according to claim 2, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on the memory map in the debugging mode.

7. The microcomputer according to claim 1, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

8. The microcomputer according to claim 2, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

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9. The microcomputer according to claim 1, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

10. The microcomputer according to claim 2, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

11. The microcomputer according to claim 1, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

12. The microcomputer according to claim 2, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

13. The microcomputer according to claim 1, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

14. The microcomputer according to claim 2, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

15. (Canceled)

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16. The microcomputer according to claim 2, said first monitor section includes:
a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and
a circuit for sending and receiving data based on said first sampling clock, and
wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

17. The microcomputer according to claim 1, said first monitor section includes a monitor RAM which is readable and writable, and when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

18. The microcomputer according to claim 2,
said first monitor section includes a monitor RAM which is readable and writable, and when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

19. An electronic instrument, comprising:
a microcomputer according to claim 1;
an input source of data to be processed by said microcomputer;
and
an output device for outputting data processed by said microcomputer.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

20. An electronic instrument, comprising:
a microcomputer according to claim 2;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

21. An electronic instrument, comprising:
a microcomputer according to claim 3;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

22. An electronic instrument, comprising:
a microcomputer according to claim 5;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

23. An electronic instrument, comprising:
a microcomputer according to claim 7;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

24. An electronic instrument, comprising:
a microcomputer according to claim 9;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

25. An electronic instrument, comprising:
a microcomputer according to claim 11;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

26. An electronic instrument, comprising:
a microcomputer according to claim 13;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

27. An electronic instrument, comprising:
a microcomputer according to claim 1;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

28. An electronic instrument, comprising:
a microcomputer according to claim 17;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

29. A debugging system for a target system including a microcomputer, said debugging system comprising:

a second monitor section which performs processing for converting a debugging command issued by a host system into at least one primitive command; and

a first monitor section which performs data transfer to and from said second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, wherein the second monitor section converts the debugging command into the primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, said first monitor section includes a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization, and a circuit for sending and receiving data based on said first sampling clock, said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

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30. The debugging system according to claim 29, said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

31. The debugging system according to claim 29, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

32. The debugging system according to claim 29, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

33. The debugging system according to claim 29, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

34. The debugging system according to claim 29, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

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35. The debugging system according to claim 29, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

36. The debugging system according to claim 29, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

37. The debugging system according to claim 29, said first monitor section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

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